**CSE 3101: COMPUTER ARCHITECTURE [2 1 0 3]**

**Pre requisites:**

* A basic course on Computers Organization and Design.

**Course Objectives:**

* To understand parallel processing and parallel computer structures.
* To understand structures and algorithms for array processors.
* To understand symmetric multiprocessor, multithreading and cluster architecture.
* To understand basics of multicore architecture.

**Course Outcomes:**

* Ability to identify different parallel computer structures and pipeline processors.
* Ability to design different SIMD interconnection networks and to describe the parallel algorithms for array processors.
* Ability to explain symmetric multiprocessor, cluster organizations and multithreading concepts.
* Ability to describe different multicore architectures.

**1.** INTRODUCTION

Organization and Architecture, Processor Organization, The Instruction Cycle, Introduction to Parallel processing, Parallel Computer Structures: Pipeline Computers, Array Computers, Multiprocessor Systems, Performance of Parallel Computers, Architectural Classification Schemes: Multiplicity of Instruction-Data streams, Serial versus Parallel Processing, Parallelism versus Pipelining (Chapter 1 Sections 1.1, Chapter 12 Section 12.1, 12.3 of Text Book 1, Chapter 1 Sections 1.1.2, 1.3, 1.3.1 to 1.3.4, 1.4, 1.4.1 to 1.4.3 of Text Book 2) (4 hrs)

**2.** PIPELINING

Principles of linear pipelining, Classification of pipeline processors, General pipeline and Reservation Tables, Instruction level parallelism: Concepts and Challenges, Data Dependences and Hazards, Control Dependences. (Chapter 3 Sections 3.1.1 to 3.1.3 of Text Book 2, Chapter 3 Section 3.1 of Text Book 3) (7 hrs)

**3.** STRUCTURES AND ALGORITHMS FOR ARRAY PROCESSORS

SIMD Computer Organizations, Masking and Data Routing Mechanisms**(2)**, Inter PE Communications, SIMD Interconnection Networks: Static versus Dynamic Networks**(1),** Mesh Connected Illiac Network**(1)(Till first sessional)**, Barrel Shifter**(1)**, Shuffle Exchange and Omega Networks**(2)**, Parallel Algorithms for Array processors: SIMD Matrix multiplication**(1)**, Parallel Sorting on Array Processors1**(1)**. (Chapter 5 Sections 5.1, 5.2, 5.2.1, 5.2.2, 5.2.4, 5.2.5, 5.3, 5.3.1, 5.3.2 of Text Book 2) (10 hrs)

**4.** MULTIPROCESSORS AND THREAD LEVEL PARALLELISM

Symmetric Multiprocessors: Organization, Multiprocessor Operating System Design Considerations, Cache Coherence and the MESI Protocol: Software Solutions, Hardware Solutions, The MESI Protocol, Multithreading and Chip Multiprocessors: Implicit and Explicit Multithreading, Approaches to Explicit Multithreading, Synchronization, Models of Memory Consistency: An Introduction, Clusters: Cluster Configurations, Operating System Design Issues, Cluster Computer Architecture, Blade Servers, Clusters Compared to SMP (Chapter 17 Sections 17.2, 17.3, 17.4, 17.5 of Text Book 1, Chapter 6 Sections 6.7, 6.8 of Text Book 3) (10 hrs)

**5.** MULTICORE COMPUTERS

Hardware Performance Issues: Increase in Parallelism, Power Consumption, Software Performance Issues: Software on Multicore, Multicore Organization, Intel x86 Multicore Organization: Intel Core Duo, Intel Core i7 (Chapter 18 Sections 18.1 to 18.4 of Text Book 1) (5 hrs)

**Text Books:**

1. William Stallings, “*Computer Organization and Architecture – Designing for Performance*”, Pearson Prentice Hall, 8th edition, 2010.
2. Kai Hwang and Faye A. Briggs, “*Computer Architecture and Parallel Processing*”, TMH Private Ltd., 2012.
3. John L. Hennessy & David A. Patterson, "*Computer Architecture: A Quantitative Approach*", 5th edition, Morgan Kaufmann, 2014.

**Reference:**

1. Er. Rajiv Chopra “*Advanced Computer Architecture (A Practical Approach)*”, S. Chand & Company Ltd, 2nd edition, 2011.

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Organization and Architecture, Processor Organization, The Instruction Cycle, Introduction to Parallel processing, Parallel Computer Structures, Architectural Classification Schemes, Pipelining, Instruction Level Parallelism, SIMD Computer Organizations, SIMD interconnection networks, Parallel Algorithms for Array processors, Symmetric Multiprocessor Organization, Cache Coherence and the MESI Protocol, Multithreading and Chip Multiprocessors, Synchronization, Models of Memory Consistency, Clusters, Operating System Design Issues, Cluster Computer Architecture, Blade Servers, Clusters Compared to SMP, Multicore Computers, Hardware Performance Issues: Increase in Parallelism, Power Consumption, Software Performance Issues: Software on Multicore, Multicore Organization, Intel x86 Multicore Organization: Intel Core Duo, Intel Core i7.

References:

1. William Stallings, *Computer Organization and Architecture – Designing for Performance (8e),* Pearson Prentice Hall, 2010.
2. Kai Hwang and Faye A. Briggs, *Computer Architecture and Parallel Processing,* TMH Private Ltd., 2012.
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4. Rajiv Chopra, *Advanced Computer Architecture (A Practical Approach), (2e),* S. Chand & Company Ltd, 2011.